

What is claimed is:

- 1 1. A method comprising:
2 selectively storing data in a memory array at
3 different densities per cell; and
4 implementing error correction depending on the
5 density of data storage.
- 1 2. The method of claim 1 including selectively
2 storing data in a memory at different densities per cell by
3 using different numbers of threshold voltage levels in a
4 given cell.
- 1 3. The method of claim 2 including using a higher
2 density mode with double the number of threshold levels as
3 a lower density mode.
- 1 4. The method of claim 3 including using a higher
2 density mode with four threshold levels and a lower density
3 mode using two threshold levels.
- 1 5. The method of claim 1 wherein implementing error
2 correction code depending on the density of data storage
3 includes determining whether data is in a higher or lower
4 density mode and if the data is in a higher density mode,
5 implementing error correction code and if the data is in a
6 lower density mode, omitting error correction code.

1 6. The method of claim 5 including using a flag to
2 indicate whether or not the data is in a lower or higher
3 density mode.

1 7. The method of claim 5 including allowing
2 overwriting when the data is stored in the lower density
3 mode.

1 8. The method of claim 7 including preventing
2 overwriting when the data is stored in the higher density
3 mode.

1 9. The method of claim 1 including allowing
2 overwriting of stored data when error correcting codes are
3 not provided for that data.

1 10. The method of claim 1 including providing a
2 multi-level memory cell array having a capacity of at least
3 four levels.

1 11. The method of claim 10 including using at least
2 two bits to represent said at least four levels.

1 12. The method of claim 11 including using one of
2 said bits as a more significant bit and the other of said
3 bits as a less significant bit.

1 13. The method of claim 12 wherein data from at least
2 two cells forms a codeword and grouping the more
3 significant bits from different cells together.

1 14. The method of claim 13 including providing more
2 significant bits in one half of a word and less significant
3 bits in the other half of a word.

1 15. An article comprising a medium storing
2 instructions that, if executed, enable a processor-based
3 system to:
4 selectively store data in a memory array at
5 different densities per cell; and
6 implement error correction depending on the
7 density of data storage.

1 16. The article of claim 15 further storing
2 instructions that, if executed, enable the system to
3 selectively store data in a memory at different densities
4 per cell by using different numbers of threshold voltage
5 levels in a given cell.

1 17. The article of claim 16 further storing
2 instructions that, if executed, enable the system to use a
3 higher density mode with double the number of threshold
4 levels as a lower density mode.

1 18. The article of claim 17 further storing
2 instructions that, if executed, enable the system to use a
3 higher density mode with four threshold levels and a lower
4 density mode using two threshold levels.

1 19. The article of claim 15 further storing
2 instructions that, if executed, enable the system to
3 determine whether data is in a higher or lower density mode
4 and if the data is in a higher density mode, implement
5 error correction code and if the data is in a lower density
6 mode, omit error correction code.

1 20. The article of claim 19 further storing
2 instructions that, if executed, enable the system to use a
3 flag to indicate whether or not the data is in a lower or
4 higher density mode.

1 21. The article of claim 19 further storing
2 instructions that, if executed, enable the system to allow
3 overwriting when the data is stored in a higher density
4 mode.

1 22. The article of claim 20 further storing
2 instructions that, if executed, enable the system to
3 prevent overwriting when data is stored in the higher
4 density mode.

1 23. The article of claim 15 further storing
2 instructions that, if executed, enable the system to allow
3 overwriting of stored data when error correcting codes are
4 not provided for that data.

1 24. The article of claim 15 further storing
2 instructions that, if executed, enable the system to
3 provide a multi-level memory cell array having a capacity
4 of at least four levels.

1 25. The article of claim 24 further storing
2 instructions that, if executed, enable the system to use at
3 least two bits to represent said at least four levels.

1 26. The article of claim 25 further storing
2 instructions that, if executed, enable the system to use
3 one of said bits as a more significant bit and the other of
4 said bits as a less significant bit.

1 27. The article of claim 26 wherein data from at
2 least two cells forms a codeword and further storing
3 instructions that, if executed, enable the system to group
4 the more significant bits from different cells together.

1 28. The article of claim 27 further storing
2 instructions that, if executed, enable the system to

3 provide more significant bits in one half of a codeword and
4 less significant bits in the other half of a codeword.

1 29. A memory comprising:
2 a memory array; and
3 a controller coupled to said memory array to
4 selectively store data in the memory array at different
5 densities per cell and to implement error correction
6 depending on the density of data storage.

1 30. The memory of claim 29 wherein said memory array
2 is a multi-level flash memory array.

1 31. The memory of claim 29 wherein said controller to
2 determine whether data is in a higher or lower density mode
3 and if the data is in a higher density mode, implement
4 error correction and if the data is in a lower density
5 mode, omit error correction.

1 32. The memory of claim 31 said controller to allow
2 overwriting when the data is stored in the lower density
3 mode.

1 33. The memory of claim 32 said controller to prevent
2 overwriting when the data is stored in the higher density
3 mode.

1 34. The memory of claim 29 said controller to allow
2 overwriting of stored data when error correcting code is
3 not provided for that data.

1 35. The memory of claim 29 said controller to use at
2 least two bits to represent four threshold voltage levels.

1 36. The memory of claim 35 said controller to use one
2 of said bits as a more significant bit and the other of
3 said bits as a less significant bit.

1 37. The memory of claim 36 said controller to group
2 the more significant bits from different cells together.

1 38. A system comprising:
2 a processor;
3 a wireless interface;
4 a memory coupled to said processor; and
5 a controller coupled to said memory to
6 selectively store data in said memory at different
7 densities per cell and to implement error correction
8 depending on a density of data storage.

1 39. The system of claim 38 wherein said memory is a
2 multi-level flash memory.

1 40. The system of claim 38 wherein said controller to
2 determine whether data is in higher or lower density mode
3 and if the data is in a higher density mode, implement
4 error correction and if the data is in a lower density
5 mode, omit error correction.

1 41. The system of claim 40 said controller to allow
2 overwriting when the data is stored in the lower density
3 mode.

1 42. The system of claim 41 said controller to prevent
2 overwriting when the data is stored in the higher density
3 mode.

1 43. The system of claim 38 said controller to allow
2 overwriting of stored when error correcting codes are not
3 provided for that data.

1 44. The system of claim 38 said controller to use at
2 least two bits to represent four threshold levels.

1 45. The system of claim 44 said controller to use one
2 of said bits as a more significant bit and the other said
3 bits as a less significant bit.

1 46. The system of claim 45 said controller to group
2 the more significant bits from different cells together.

1 47. The system of claim 38 wherein said wireless
2 interface includes an antenna.

1 48. The system of claim 47 wherein said wireless
2 interface includes a dipole antenna.